DESIGN OF TERNARY LOGIC BASED ON RERAM CROSSBARS

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ABSTRACT

Implementing logic within ReRAM crossbar is an attractive approach to overcome the memory wall in conventional von Neumann architectures. Compared to binary logic, the ternary logic can reduce area and power overhead with enhanced computing speed. In this paper, a ternary logic design based on ReRAM crossbars is proposed. Experimental results show that the proposed ternary logic gates have better performance in terms of switching speed, area, and power as compared to the previously published IMPLY and MAGIC designs.

INTRODUCTION

With the explosive growth of data, the conventional von Neumann architecture encountered memory wall with prolonged latency and increased power consumption due to massive data movement between memory and processing unit [1]-[5]. The traditional digital computing system is binary logic where only two logic values are used, which may occupy more chip area and slower down the processing speed. Furthermore, the conventional silicon CMOS is approaching fundamental physical limitations due to exacerbated subthreshold leakage currents in deep-nanoscale regime [6]-[8]. New computing paradigm that can overcome memory wall and perform logic operations more efficiently is highly desirable for future data-intensive application.

The logic operations can be performed within the high-dense ReRAM crossbars, which can eliminate the massive data transfer in conventional von Neumann architecture. Recent works on logic based on ReRAM crossbars, such as material implication (IMPLY) [2] [3] and memristor aided logic (MAGIC) [4] [5], focus on binary logic operations. The inputs and outputs in the MAGIC and IMPLY circuits are represented by the single-level cells (SLCs) within one crossbar. Only one type of Boolean operation is allowed in either MAGIC or IMPLY with limited fan-ins/fan-outs.

Ternary logic uses three logic values to process information, thereby can reduce the area overhead and enhance the computing speed compared to binary logic. However, ternary logic implementations are still limited to the conventional von-Neumann architecture [9]. Implementing ternary logic on ReRAM crossbars remains a great challenge.

In this work, a new ternary logic implemented with ReRAM dual-crossbars is proposed. In the proposed ternary logic, both inputs and outputs are represented by the resistance of multi-level ReRAMs. The carbon nanotube transistors (CN-MOSFETs) which can be integrated with ReRAM [6] are employed in peripheral circuitry for reduced footprint and energy consumptions. Two ternary logic gates supporting multiple fan-ins/fan-outs are realized. Experimental results show that the proposed ternary logic gates have better performance in terms of switching speed, area, and power as compared to the previously published IMPLY and MAGIC designs.

TERNARY LOGIC DESIGN ON RERAM CROSSBARS

A ternary logic design based on the ReRAM dual-crossbars is proposed as illustrated in Figure 1. The three logic values 0, 1, and 2 are represented by the high resistance state (HRS), medium resistance state (MRS) and low resistance state (LRS) of multi-level ReRAM, respectively. Two-variable ternary gates NMAX and MAX (also known as ternary NOR and ternary OR gates) along with several unary operators can form the functionally complete algebra of ternary logic [10]. In this paper, the ternary NMAX and MAX gates (with multiple fan-ins and fan-outs) are realized within the dual-crossbar structure as shown in Figure 1.

The truth tables of NMAX and MAX are shown in Figure 2(a). The implementation of the NMAX and MAX gates are illustrated in Figure 2(c) and (d), respectively, which can be directly mapped to the dual-crossbar structure in Figure 1. When mapping the NMAX and MAX gates into the dual-crossbar structure, the inputs are required to be aligned in the same column while the corresponding output is allocated in the other crossbar.

Taking the NMAX gate in Figure 2(c) as an example, the input ReRAMs (A and B) store the ternary resistances while the output ReRAM is initialized to HRS prior to operation. To initiate the operation, proper peripheral voltages V_{cond} and V_{WR} are applied. The input ReRAMs and the reference resistor (R_T) form a voltage divider, driving the following standard ternary inverter (STI) [9]. The STI can output three discrete voltage levels (V_{so}) based on different input voltages (V_{si}). Considering

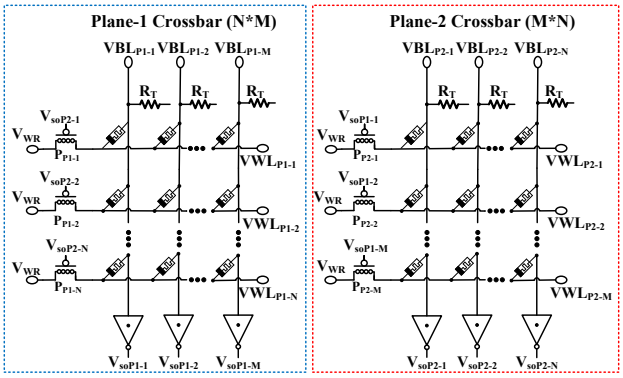

Figure 1: The proposed ternary logic based on ReRAM dual-crossbars.

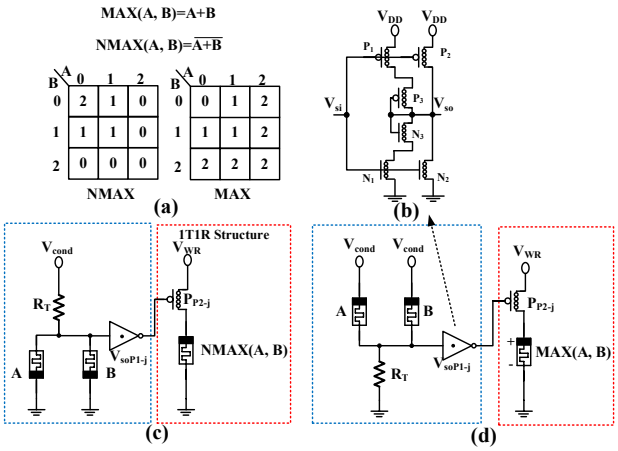

Figure 2: Implementation of NMAX and MAX gate. (a) Truth tables. (b) Schematic of STI circuit. The flat-band voltages of N_1, P_1, N_2, P_2, N_3, P_3 are set to be 0V, 0V, 0.45V, -0.45V, 0.45V, and 0V, respectively. (c) Schematic of the NMAX gate. (d) Schematic of the MAX gate.

the high driving strength and small device footprint of CN-MOSFETs [7] [8], the carbon-based STI is implemented as shown Figure 2(b) to preserve the high switching performance and integration density of ReRAM crossbars. Proper flat-band voltages of different transistors are applied to achieve the desirable output voltages (V_{so}) of STI. Three discrete voltages of V_{so} drive the gate of p-channel CN-MOSFET in the 1T1R structure as shown in Figure 2(b). The compliance current flowing through the 1T1R is changed with V_{so} [1]. The output ReRAM is conditionally maintained at HRS or switched to lower resistance states depending on the input scenarios.

Given that the inputs are aligned in one crossbar plane, multiple NMAX or MAX gates on different columns can be executed in parallel, which generate the outputs along a column in the other crossbar plane. By isolating the inputs (located in Plane-1 with blue-line block) and outputs (located in Plane-2 with red-line block) of the NMAX and MAX gates into different crossbar planes, multiple fan-ins and fan-outs are supported by adjusting the control signals of V_{cond} and V_{WR} as shown in Figure 2. When cascading multiple NMAX or MAX gates for realizing a complex ternary logic function, the inputs and outputs can be allocated alternately in two crossbar planes.

EXPERIMENTAL RESULTS AND DISCUSSION

The simulation waveforms of the NMAX gate are illustrated in Figure 3. HSPICE simulation is performed based on the physics-based ReRAM Verilog-A model [11] and Stanford University Virtual Source GAA-CN-MOSFET model [12] [13] assuming a 16nm technology node with a supply voltage of 0.7V. The HRS and LRS values are assumed to be 1MΩ and 5kΩ, respectively [11]. V_{cond} is 0.7V and V_{WR} of 1T1R is 1.3V. To guarantee the correctness of transition of output ReRAM for different input data scenarios in the presence of process variations, the reference resistor (R_T) and MRS are selected to be 35kΩ and 60kΩ, respectively. Provided that at least one of the inputs is at LRS (logic '2'), the output is maintained at HRS (logic '0') as shown in Figure 3(a). Alternatively, the output is transitioned to LRS (logic '2') if both inputs A and B are at HRS (logic '0'), as shown in Figure 3(b). Other cases yield an output of MRS (logic '1') from Figure 3(c).

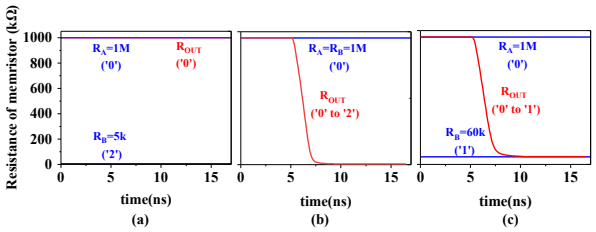

Figure 3: Simulation waveforms of NMAX gate. (a) Input A is at HRS ('0') and input B is at LRS ('2'). (b) Both of the inputs A and B are at HRS ('0'). (c) Input A is at HRS ('0') and input B is at MRS ('1').

The worst-case delay and average power consumption of MAGIC, IMPLY and proposed ternary logic are listed in Table I. The delay is measured under 1.3V operating voltage for V_0 [4] in MAGIC, 1.3V voltage for V_{set} [2] in IMPLY, and 1.3V voltage for V_{WR} in the proposed ternary logic for the worst case. The worst-case delay for IMPLY is both of the inputs are at HRS (logic '0'). The worst-case delay for MAGIC is the inputs are at HRS (logic '0') and LRS (logic '2'). The worst-case delay for the proposed ternary logic is the inputs are at HRS (logic '0') and MRS (logic '1') for MAX gate and both of the inputs are in MRS (logic '1') for NMAX gate. The power consumption is measured in 6.5ns clock period and calculated by averaging over all input combinations.

As listed in Table 1, the proposed ternary logic provides the smallest switching delay since the output ReRAM resistance swing is reduced as compared to the

previously published binary MAGIC and IMPLY with full resistance swing. The delay of the proposed ternary NMAX gate is reduced by 9.23% and 28.37% compared to MAGIC and IMPLY logic gates, respectively. Due to the lowest transition probability of output (from HRS to MRS or LRS), the proposed ternary NMAX gate consumes the lowest power among the logic designs that are evaluated in this study. The power consumption of the proposed ternary NMAX gate is reduced by 53.58% and 73.22% compared to MAGIC and IMPLY logic gates, respectively.

Table 1: Delay and power comparison

Logic Designs	***MAGIC***	***IMPLY***	***MAX***	***NMAX***
Delay (ns)	5.09	6.45	4.67	4.62
Power (μW)	74.43	129.00	110.27	34.55

CONCLUSION

In this work, a new ternary logic implemented with ReRAM dual-crossbars is proposed. In the proposed ternary logic, both inputs and outputs are represented by the resistance of multi-level ReRAMs. Two ternary logic gates supporting multiple fan-ins/fan-outs are realized. Experimental results show that the proposed ternary logic has better performance in terms of switching speed, area, and power as compared to previously published IMPLY and MAGIC designs. Future work will be focusing on the implementation of unary operators in peripheral circuits to form the functionally complete algebra of ternary logic and exploring the real-world applications of ternary logic especially on ternary arithmetic operations and database ternary bitwise operations.

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